ABSTRACT OF THE DISCLOSURE

In a clock-synchronized serial communication device, a counter counts pulses in a communication clock signal. When the count reaches 8, the counter sets a start signal. With this start signal, a pulse generator outputs the first to fourth signals successively. Received data stored in a receiving shift register is transferred to a received-data processing circuit synchronously with the first signal. The received data is further transferred to a timer-setting value register as a timer-setting value synchronously with the second signal. A timer present value is output from a timer present value register synchronously with the third signal. The timer present value is further written into a transmitting shift register as transmission data synchronously with the fourth signal.